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Efficient And Advance Routing Logic For Network On Chip

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ABSTRACT –
VLSI technology has improved in integrating several Intellectual Properties (IP's) on the same chip. Connections between these IP's are the major issue and the Network on Chip (NoC) plays an important role in connecting these IP's. NoC has a high level of modularity, flexibility and throughput. The NoC comprises of routers, network interfaces and links allowing communication between the processing element. The path to be traversed for a data packet between source and a destination through the routers is defined by the routing algorithm. A new routing logic for Network on Chip which can handle the fault occurring during runtime is presented in this paper. It is based on error detection mechanism suitable for dynamic NoC's, where the number and position of the element or faulty blocks vary during runtime. The advance reliable network consists of router with four ports that has separate routing logic block and error correcting mechanism. The proposed reliable routing protocol and router architecture is used to connect the IP cores to provide an efficient routing logic. The performance of the router architecture is analyzed in different structural conditions thus proving to avoid both dead lock and live lock.

Keywords—Network on Chip (NoC), System on Chip (SoC), Cyclic Redundancy Check (CRC), dead lock, live lock

I. INTRODUCTION

The wiring modules on chip is not a viable solution in the billion transistor chips for the future. The Network on Chip (NoC) [4] is a good solution to support communication on System on Chip. NoCs encounter many advantages (performance, structure and modularity) towards global signal wiring. A chip employing an NoC consists of a set of network clients such as DSP, memory, peripheral controller, custom logic that communicate on a packet base instead of using direct connections. Several modules (network client) placed at fixed locations on the chip can exchange packets in the common network. This provides very high flexibility, as no route has to be computed before allowing components to start communicating. The Components just send packets, and it does not care on how the packets are routed in the network. NoC is viewed as the critical key to prevail over the trouble that will arise because of the growing size of the chip. The NoC architecture is characterized by the number of routers which is linked to processing elements in the array, the bandwidth of the communication channels between the routers, the topology of the network and the mechanism used in data transmission

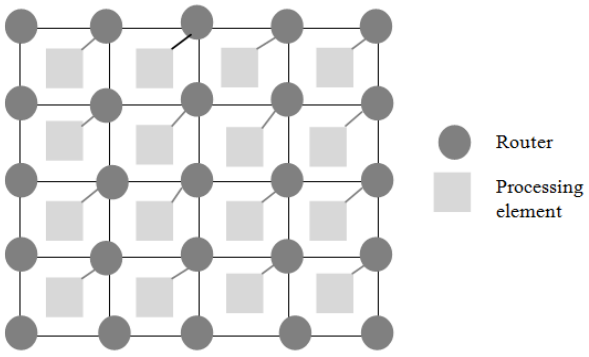


Fig.1. Network on Chip

The topology [9] of the network is defined through the arrangement of routers and processor connection on the device. The most commonly used topology is the 2-D mesh topology, which looks like an arrangement of tiles as shown in Fig.1. NoC is built with routers and processing elements and/or IPs

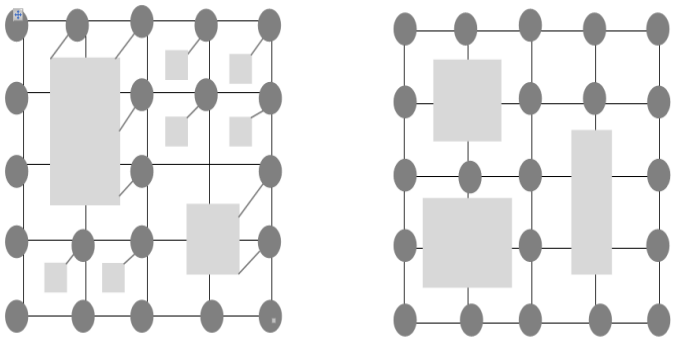
.The routers consists of FIFO buffers, control logic and arbiter. Buffers are used for storing the data in order to forward the message in First In First Out basis. The main function of the control logic is to synchronize the data transmission in the correct order to reach the destination from the source via particular router. The work of the arbiter is to avoid the congestion of data due to traffic, whereas the finite state machine in the arbiter forwards the data in a Round-robin scheduling. The processing element is connected to the router via the wrapper. There are several types of routing techniques used in NoC namely circuit switching, store and forward, virtual cut through, worm hole etc [4]. The routing logic used in routing techniques is classified in to two types namely: deterministic and adaptive routing logics.

II. RELATED WORKS

In order to meet the real time applications the trend of embedded system has been moving towards Multiprocessor System on Chip (MpSoC), where the number of SoC is more. Increasing the number is becoming a burden for connecting medium. Connecting the SoC's through NoC gives an effective connection between the peripherals. The peripherals were connected through a shared bus in the earlier period, which can be either single or multiple shared busses connected using bypass bridges [12] and point-to-point connection between the peripherals [4]. This development of connection led to network on chip, where the peripherals are connected by splitting into certain sub circuits via NoC [2]. One of the main challenges of NoC is that it has to face the dynamically placed reconfigurable devices which later emerged into dynamic NoC [1]. Configurable network [11] was designed to obtain dynamic reconfiguration of FPGAs. The NoC is further modified to improve the performance and manage the dynamically placed modules using the inclusion of certain switching techniques [8] [6]. Now the focus is towards the data transmission with minimum error that can be achieved by the inclusion of error correcting techniques in the router [10]. In [9] error correcting code is included only on any two ports of the router among the four, and it is further incorporated with all the four ports to improve the performance of NoC [8]. The path between the source and the destination is defined through routing algorithms. The most suitable routing algorithm for mesh network is *XY* algorithm, but it cannot be used to avoid both dead lock and live lock. To overcome the above limitations, adaptive routing logic is used that updates the information about the neighbouring router [2]. Adaptive *XY* routing algorithm includes the concept of Odd-Even algorithm [3] and *XY* algorithm well suited for a NoC which uses dynamically reconfigurable devices [2]

III. MOTIVATION

The routing technique and the router structure of NoC are developed in order to fulfil the requirements of communication between the peripherals and trade off between power, area and time. NoC with five port router is designed to manage dynamically the change of modules is Dynamic NoC (DyNoC) [1] which is depicted in Fig.2. (a). DyNoC obeys *XY* algorithm and it cannot be used to overcome both live lock and dead lock. Further to overcome the architectural limitations a four port router is designed where the modules links to the network replacing one or more routers. Such type of NoC's are said to be as Configurable NoC's (CONOCHI) [11]. The modules are linked to only one of the router ports hence live lock and dead lock occurs. To improve the design of router, the modules are connected using Communication Switches (CU) [7], where the input buffers are absent. The CU is classified in to two types namely classic CU and to-give-way CU. Both the types work in same way under normal circumstances. To overcome the bottleneck in receiving the flits due to the absence of input buffers, the switching networks is used which obeys priority-to-the-right rule named as QNoC [6] which is depicted in Fig.2 (b). Live lock and dead lock can occur in QNoC if a fault occurs in the connection between the modules and routers. Integration of loopback module in the router can redirect the message through another port if it finds any fault in its transmitting path. This structure of the switch with loopback module is discussed as RKT NoC [8]. It also includes correction of errors occurring in the transmitted data using hamming codes. The limitation is that even if the path and the transmitting data is processed correctly the architecture of the hamming coder is prone to fault [2] and it cannot be used for burst error correction of messages. To avoid both dead lock and live lock reliable router architecture is proposed by replacing the hamming coder by cyclic redundancy code that can detect burst errors suitable for correcting errors under different traffic conditions



(a) (b)

Fig.2. (a) Dynamic NoC. (b) QNoC

IV. PROPOSED ROUTER ARCHITECTURE

A Reliable switch architecture to overcome both live lock and deadlock is proposed in this paper. The proposed architecture has four ports suitable for a 2-D mesh NoC and each port consists of error correction blocks, buffers and routing logic blocks as shown in Fig. 3. The PEs and IPs can be linked directly to any side of a router. Therefore, there is no particular connection port for a PE or IP. In this four-port reliable switch architecture, an IP can replace several switches by having several input ports and hence be strongly connected to the network

A. *Error Correction*

Transmission of data without any error in the Network on Chip ensures integrity of data. To guarantee error free transmission of messages, the error correcting techniques is included in the switch to avoid both routing error and data error. This paper uses cyclic redundancy for data error checking, which has the tendency to check burst errors. If error occurs then it sends a negative acknowledgement to the source requesting for retransmission. Each switch is identified by a unique address mentioned in matrix form. When a message is passed from one IP core to another IP core via switch, it checks the status of the flits received. Flits received through the loop back mechanism indicate that the router ahead is faulty. The flits routed by XY algorithm states that therouter ahead is not faulty. If adaptive XY algorithm is used then the flits are received to bypass the faulty router. The availability of the next router is determined by checking the status of the availability signal along the diagonal direction. Thus the routing error detection mechanism is highly suitable to avoid both dead lock and live lock, Deadlock is a situation that occurs when a packet is waiting for an event that can never happen because of circular dependence on resources**.** Livelock, on the other hand, is a configuration of the network in which packets continue to move, but never reach their destination.

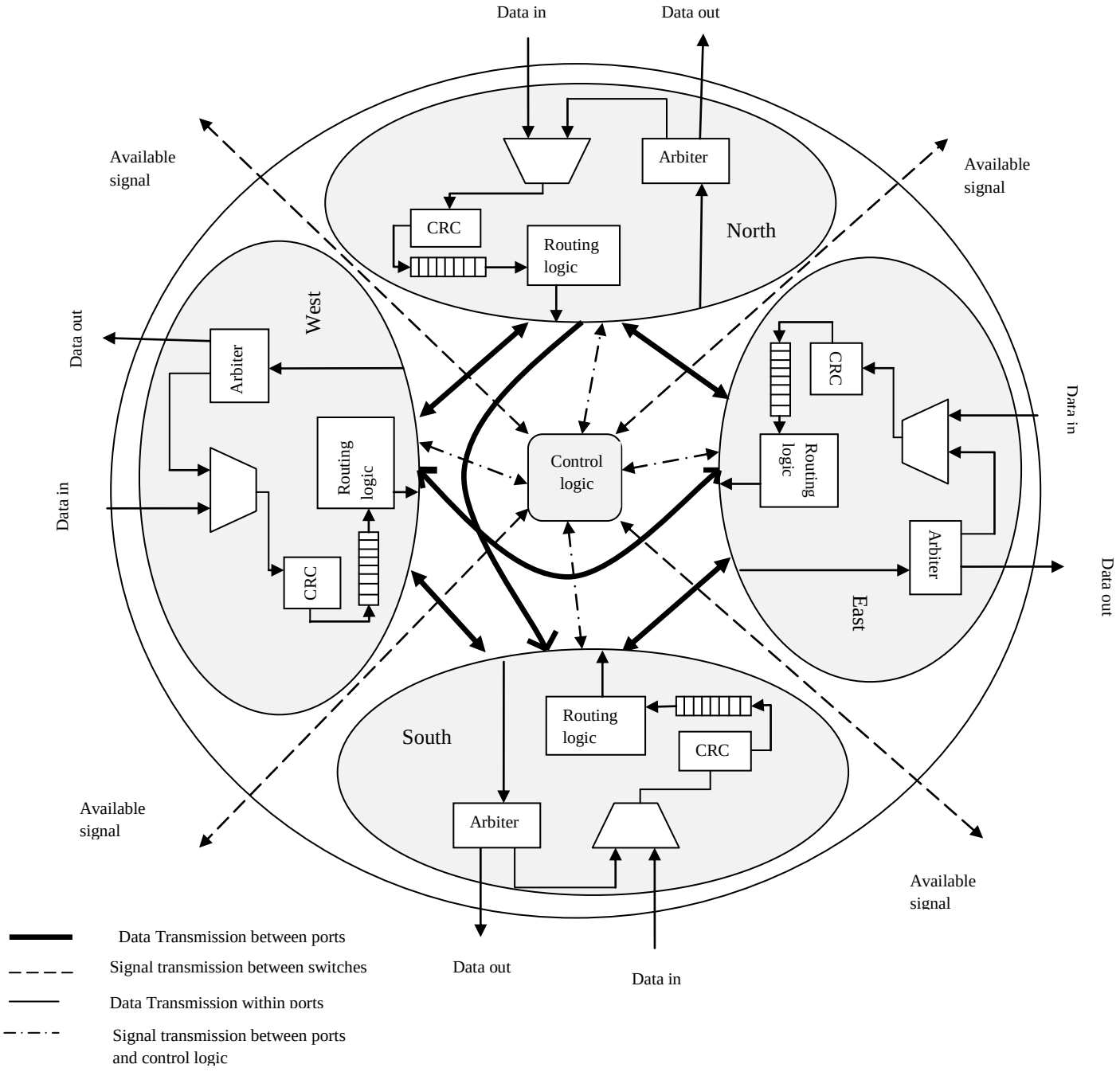


Fig. 3. PROPOSED ROUTER ARCHITECTURE

B.*Routing Logic*

Routing acts as the backbone to avoid deadlock and live lock. The routers have the address in the matrix format i.e., it is defined by its xy coordinated. Hence it is a mesh network where each and every router is addressed with its position. It uses a well suited XY algorithm added with some adaptiveness to avoid deadlock and live lock. When the network starts to send messages from the source node to the destination, initially it compares its own x coordinate position with the destination position and move either towards its right or left if and only if the neighbour router is available, If the router in its corresponding path is unavailable, it compares the y coordinates position and moves either to the top or to the bottom. Alternately it checks the x and y coordinate until it reaches the condition that both the current router location is

equal to the destination router location. It is because the address of the IP core is the address of the router to which it is connected. The routing logic follows a loopback mechanism to overcome those locks. The crossbar switch in the arbiter sends the data to the next switch or to the input of same multiplexer of the same port in accordance to the availability of signal given by the control logic. The switch forwards the data to next switch. If the following switch is under fault or under any traffic condition, it does not give any request for receiving the data so the crossbar switch in the arbiter sends the data to the loopback path instead of sending it to the output line of the switch. Thus this routing logic highly avoids both deadlock and live lock.

V. PERFORMANCE EVALUATION

Evaluation of the router architecture is performed with the help of transmitting 24bit data through the router, which consists of four flits and buffer storing two flits per router. With respect to this condition, inputs are applied to the ports of the router and the parameters determining quality of service like throughput, latency and number of logic elements used is evaluated.

A. *Latency*

Latency is the time taken for a data packet to reach its destination from the source. Thus this router uses store and forwarding technique. Due to this technique the time taken for transmitting the data depends on the no of flits (F_{no}) to which the data is segmented. The router also takes some time to check the data using CRC. Hence the time taken for this process (T_{CRC}) is also included in calculation. Apart from including the cycles needed for the two process, an addition of three more cycle is need for a data to cross the router. One cycle for the routing logic, another for flits arriving t the multiplexer and one for flits leaving the arbiter. The equation including the above parameters is given by 1.

$$\text{Latency}_{\text{router}} = F_{no} + T_{CRC} + 3 \quad (1)$$

B. *Throughput*

Maximum traffic that a network can handle is throughput. It depends on the width of the data (W), frequency under which the data is transmitted (f_t), number of IPs connected (IP_{nos}) to it and rate of inputs given to the router ($R_{i/p}$) as given by 2.

$$\text{Throughput} = IP_{nos} \times W \times f_t \times R_{i/p} \quad (2)$$

TABLE 1. PERFORMANCE COMPARISON

Rate of injection input	Cyclone III			Cyclone IV		
	Processing Elements (Logic Elements)	*Frequency (MHz)*	*Maximum Throughput (Gbits/s)*	*Processing Elements (Logic Elements)*	*Frequency (MHz)*	*Maximum Throughput (Gbits/s)*
0.369	3215	531.35	112.82	3354	539.47	114.67

Consider a single router that can store two flits out of the four flits of the data which is transmitted. The throughput is calculated by estimating the rate of input injection as 0.369 and tabulated thus the calculation of throughput and latency using Cyclone III and Cyclone IV is tabulated in Table 1.

VI. CONCLUSION

The proposed router architecture in this paper includes an advanced routing logic and burst error correction mechanism. So it is well suited for the network under heavy traffic conditions. Increasing the number of intellectual properties increase the traffic and this router connection in NoC will be useful to detect and correct the errors. This switch also gives a better solution to avoid deadlock and live lock conditions. This switch can be analyzed for various traffic conditions and the performance can be evaluated for the entire network architecture.

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